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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/753,673 | 01/07/2004 | I-Sheng Liu | M-15281 US | 6785 |

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|---|---|
| MONDT, JOHANNES P | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 3663 | |

DATE MAILED: 08/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/753,673 | LIU ET AL | |
| | Examiner | Art Unit | |
| | Johannes P. Mondt | 3663 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *11 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1 and 3-14* is/are pending in the application.

4a) Of the above claim(s) *10-14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/11/06 has been entered.

### *Response to Amendment*

Amendment filed 7/11/06 with said RCE forms the basis for this office action. In said Amendment applicants substantially amended all elected pending claims through substantial amendment of claim 1. Comments on Remarks submitted with said Amendment are included below under "Response to Arguments".

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. ***Claims 3-9*** recite the limitation "claim 2" in lines 1. There is insufficient antecedent basis for this limitation in the claim because claim 2 has been cancelled.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. ***Claims 1, 3, 6, 7 and 9*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al (5,912,842) in view of Chindalore et al (US 2004/0070030 A1). Referring to the noted indefiniteness under 35 U.S.C. 112, second paragraph, it is assumed in the rejections of claims 2-9 that the wording "claim 2" in claims 3-9 may be replaced by "claim 1".

*On claim 1: Chang et al teach* a two-transistor PMOS memory cell (see title and abstract, first sentence), comprising: a PMOS select transistor 40b (col. 4, l. 2 and Figure 3) having a drain and source 50 and 48, respectively (cf. col. 4, l. 3-7), formed as separate P+ diffusion regions in an N- well 42 (col. 4, l. 2); a PMOS floating gate transistor 40a (cf. col. 4, l. 1) having a drain and a source 46 and 48 (cf. col. 4, l. 6-9) formed as separate P+ diffusion regions in the N- well, wherein the P+ diffusion region 48 that forms the floating gate transistor's drain is the same P+ diffusion region that forms the select gate transistor's source (col. 4, l. 4-6).

*Chang et al do not necessarily teach an N implant* underlying the P+ diffusion region that forms the floating gate transistor's drain with lateral extent no greater than that of said P+ diffusion region.

*However, it would have been obvious to teach an implant underlying the heavily doped drain diffusion region of the floating gate in view of Chindalore et al,* who, in a patent on a floating gate (see paragraphs [0003] and [0021]) for non-volatile memory devices, -hence analogous art, teach in particular the prevention of punch-through through the inclusion of a halo implant 46 underlying the *drain* region 54 of said floating gate 32 *only* (cf. [0014]), said halo implant being of opposite conductivity type in comparison to said drain region, said halo 46 having a lateral extent no greater than that of drain 54, as can be seen from Figure 3, wherein the lateral extent of region 46 is limited on the gate side by distance 47 (say "D") (cf. [0024]) from the normal at the gate's edge, which is the depth in the substrate measured from the upper main surface (say "H") multiplied by the tangent of the angle of implant $\theta$ (cf. [0024]), i.e., $D = H\ tg(\theta)$, while said lateral extent of region 46 is limited from the other side, i.e., the one most distant from the gate's edge, by the ion implantation step for region 54, at a position at a markedly greater depth ("H") related to the distance $\Delta$ of said position to region 24 according to $\Delta = H\ tg(\theta)$. Therefore, the lateral extent of 46 is less than that of drain 54 (because $D<\Delta$).

It is exactly the hot-carrier injection in the floating gate stacks in both Chang et al and Chindalore et al that prompts the inclusion by Chindalore et al of the implant of conductivity type opposite to that of source and drain on the drain side (see [0014]),

*motivation* for the inclusion of the teaching by Chindalore et al in the invention by Chang et al exists and derives from the resulting additional protection against punch through in floating gates. Because the hot carrier injection is specific to the floating gate one of ordinary skills in the art would consider it obvious to include one halo region underlying the drain of the floating gate stack 10 in Chang et al and nowhere else.

Finally, a consistent overall interchange of n-type and p-type conductivity in Chindalore is within the scope as claimed (see claims, page 7).

*On claim 3:* the drain of the PMOS select transistor 50 couples to a bit line BL0 of a memory array 70 (cf. col. 5, l. 1-15), and a select gate 40 b of the PMOS select transistor couples to a word line WL0 (loc.cit.) of the memory array 70.

*On claim 6:* the memory cell is configured such that the floating gate transistor is *capable* of being programmed using band-to-band tunneling because a thin tunnel oxide layer 56 (col. 31-33) is included while the two transistors are PMOS transistors. Furthermore, in reference to the claim language referring to "may be programmed", intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963).

*On claim 7:* The capability for Fowler-Nordheim tunneling is implemented in a preferred embodiment in Chang et al (col. 5, l. 63 – col. 7, l. 51). Furthermore, in reference to the claim language referring to "may be programmed", intended use and

other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963).

*On claim 9:* the thickness of the implant of opposite conductivity type underlying the heavily doped drain diffusion region that forms the floating gate transistor's drain in the combined invention includes a range that overlaps with the range as claimed, because the lateral excursion of said implant by Chindalore is 500 Angstroms (see [0024]) while the implant angle θ is between 20 and 60 degrees (see par. [0024]), while for all implant angles less than 26 degrees the depth is more than twice said lateral excursion, i.e., more than 1000 Angstroms. A *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003).

2. ***Claim 4*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al and Chindalore et al as applied to claim 2 above, and further in view of Chang et al (5,687,118). In the combined invention by Chang et al and Chindalore et al a floating gate 54 is formed in a first polysilicon layer (col. 4, l. 8-9). Neither Chang et al nor Chindalore et al necessarily teach the control gate of the PMOS floating gate transistor to be formed of polysilicon. However, it would have been obvious to include the further

limitation on the material constitution of said control gate as claimed in view of Chang et al (5,687,118) ("Chang 2" henceforth) who teach in very closely related art the material constitution of the control gate to be polysilicon as well (cf. col. 11, l. 46-56). *Motivation* to include the teaching by Chang2 at least stems from the economy to use the same material for extremely similar structures in the same invention. Furthermore, Applicant is reminded in this regard that it has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. *In re Leshin* 125 USPQ 416. Chang2 proves that polysilicon for the material selection of the control gate in a floating gate transistor is generally understood to be suitable.

3. ***Claim 5*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al and Chindalore et al as applied to claim 2 above, and further in view of Yaegashi et al (US 2002/0098638 A1). As detailed above, claim 2 is unpatentable over Chang et al in view of Chindalore et al *Although Chang et al teach* the memory cell to include a single polysilicon layer containing a floating gate (col. 4, l. 9-11 and Figure 3, *neither Chang nor Chindalore necessarily teach* the further limitation as defined by claim 5. *However, it would have been obvious* to include said further limitation in view of Yaegashi et al who teaches a back-gate as control gate to facilitate erase operations (see paragraph [0347] and Fig. 71). *Motivation* to include the teaching by Yaegashi et al in the invention thus derives at least from facilitating an operation that is routinely performed by any memory cell including that of the invention.

4. ***Claim 8*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al and Chindalore et al as applied to claim 2 above, and further in view of Prall et al (5,345,104). As detailed above, claim 2 is unpatentable over Chang et al in view of Chindalore et al. Neither necessarily teach the further limitations of claim 8. *However, it would have been obvious to include the further limitation as defined by claim 8 in view of Prall et al*, who, in a patent on creating halo regions in a MOSFET with floating gate within the context of a flash memory cell, - hence closely related art, teach the thickness of the drain region 18 of the floating gate's transistor to be approximately 1000 Angstrom = 0.1 micron (cf. col. 3, l. 55-60), which is in the range as recited in claim 8, considering the verbiage "approximately". Applicant is furthermore reminded that a *prima facie* case of obviousness typically exists when the ranges of a claimed quantity overlap the ranges disclosed in the prior art or when the ranges of a claimed quantity do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003).

### ***Response to Arguments***

Applicant's arguments filed 7/11/06 have been fully considered but they are not persuasive. In particular, the following comments are provided in response to applicants' arguments on those elected claims still in the application:

(a) Applicants allege that the purpose of applicants' implant would be destroyed by the angled implant of Chindalore. However, this is interesting but irrelevant for the validity of the rejection under 35 USC 103(a), for which the requirement is whether or

not it would have been obvious to include the teaching by Chindalore in the invention by *Chang*. The arguments in the previous office action on page 3 argue that it indeed would have been obvious. These arguments are not addressed in applicants' Remarks.

(b) Applicants' additional argument is the allegation that "Chindalore makes no teaching or suggestion for an implant having the lateral extent limitation of claim 1". This additional argument is not persuasive because the lateral extent of region 46 is limited on the gate side by distance 47 (say "D") from the normal at the gate's edge, which is the depth in the substrate measured from the upper main surface (say "H") multiplied by the tangent of the angle of implant $\theta$, i.e., $D = H\ tg(\theta)$, while said lateral extent of region 46 is limited from the other side, i.e., the one most distant from the gate's edge, by the ion implantation step for region 54, at a position at a markedly greater depth ("H") related to the distance $\Delta$ of said position to region 24 according to $\Delta = H\ tg(\theta)$. Therefore, the lateral extent of 46 is less than that of 54 ($D<\Delta$). Chindalore thus meets said limitation.

Therefore, applicants' arguments do not appear to be persuasive based on the present claim language.

The rejections above were prompted by these considerations.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JPM
August 5, 2006

Patent Examiner:

Johannes Mondt (Art Unit: 3663)